FIG. 1A

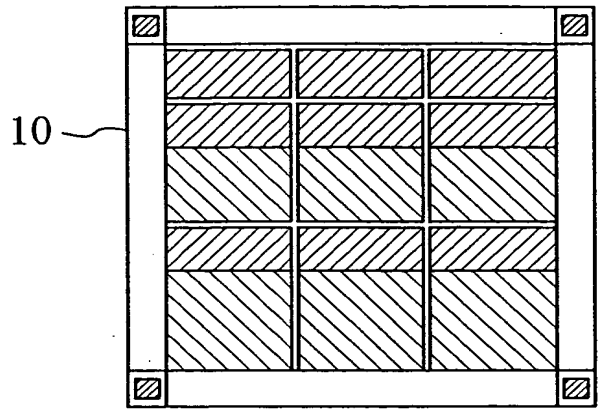

FIG. 1B

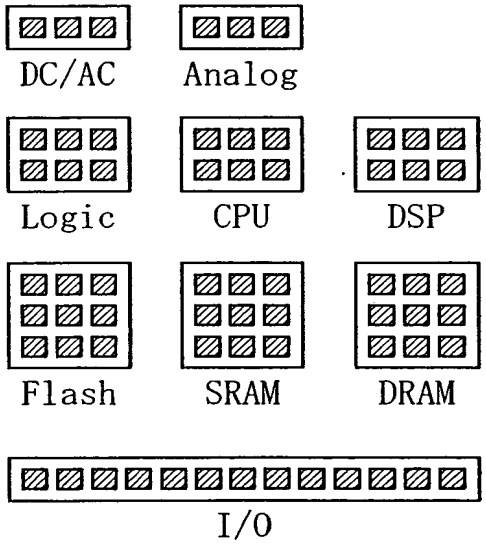

FIG. 1C

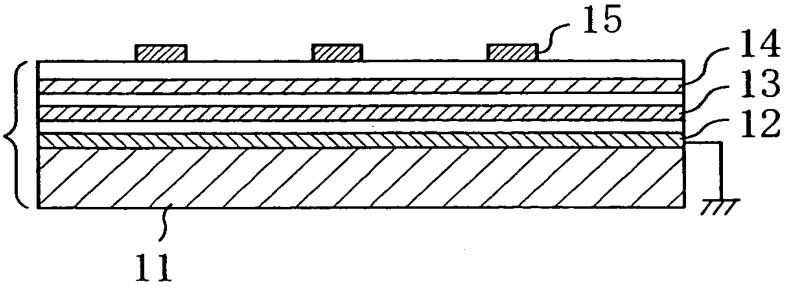

FIG. 2

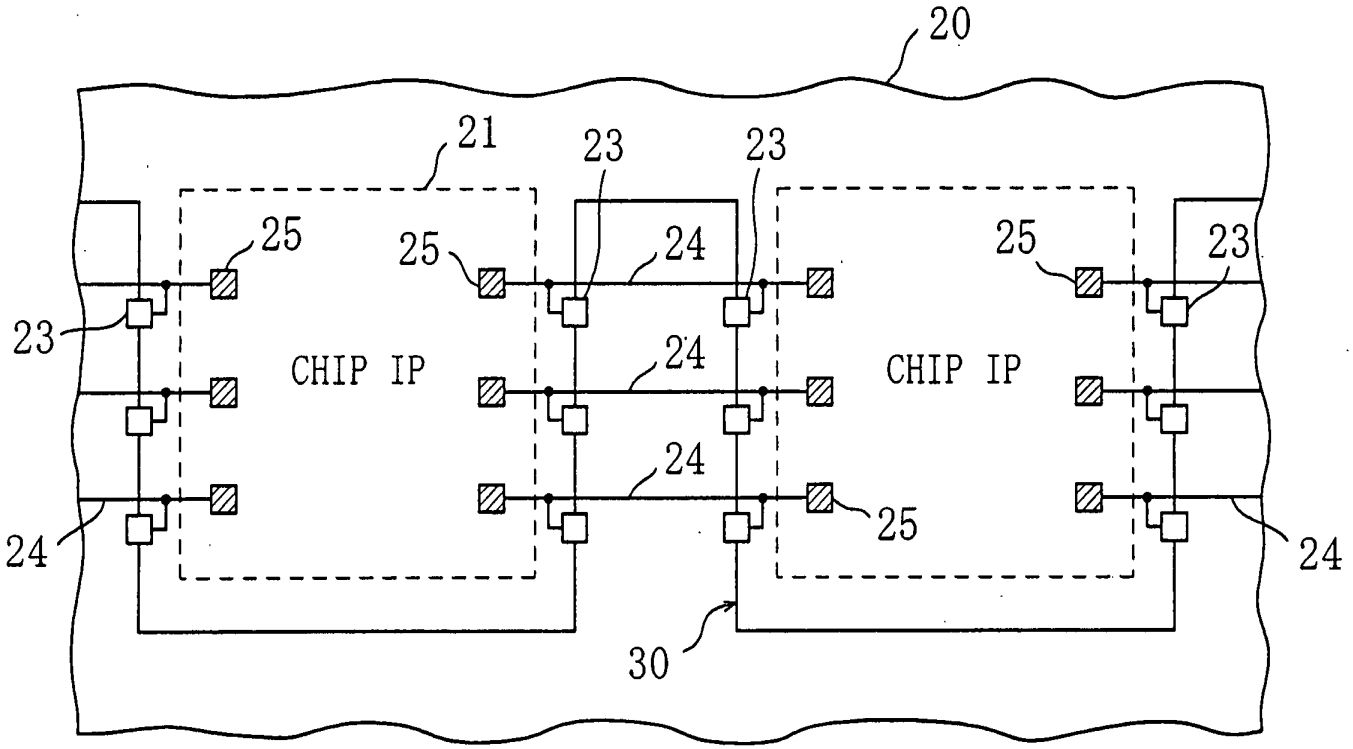

FIG. 3A

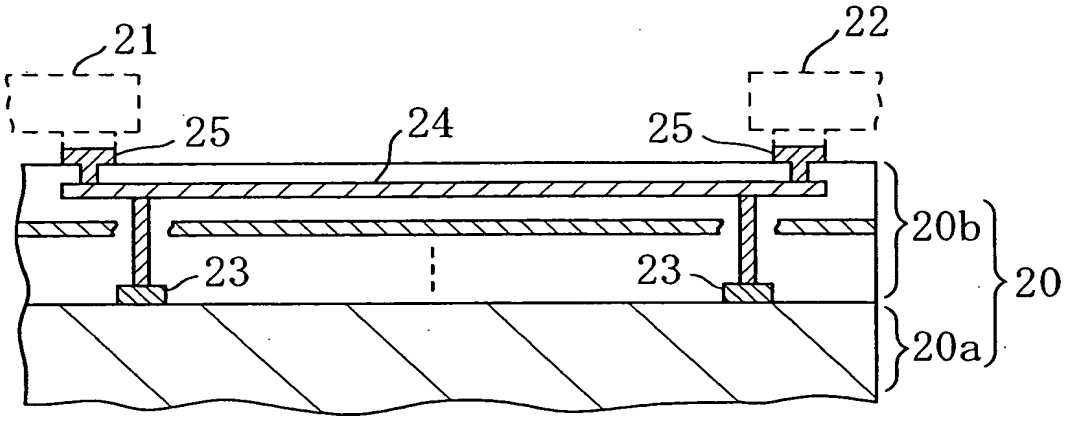

FIG. 3B

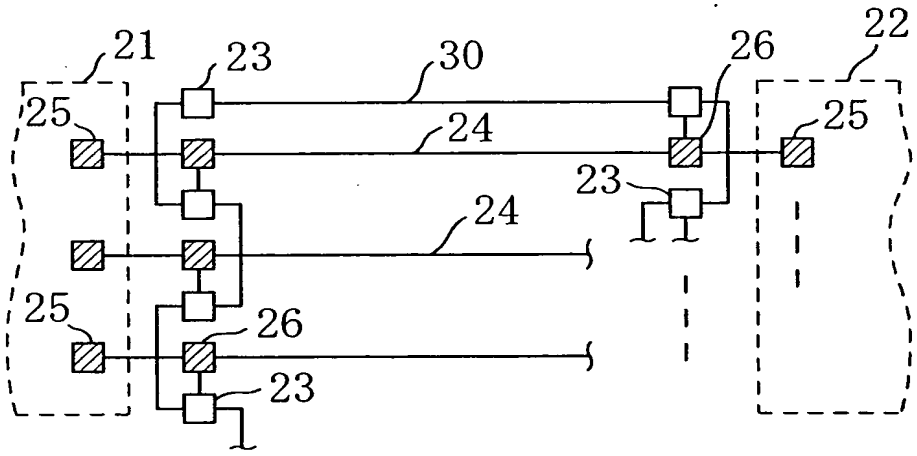

FIG. 4

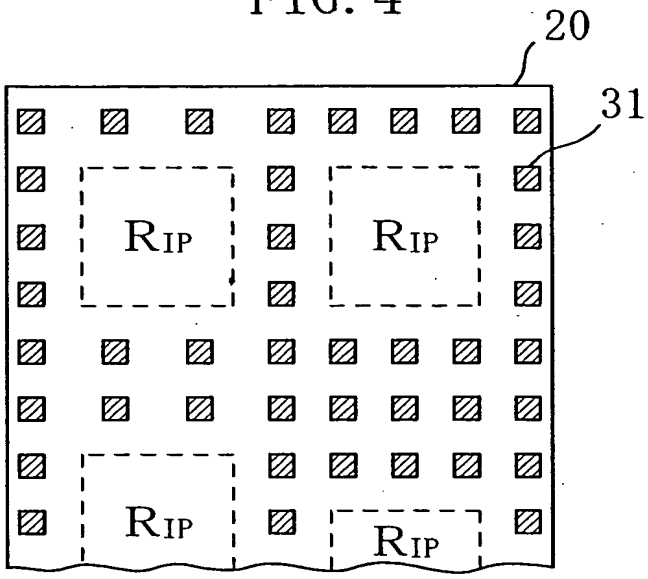

FIG. 5

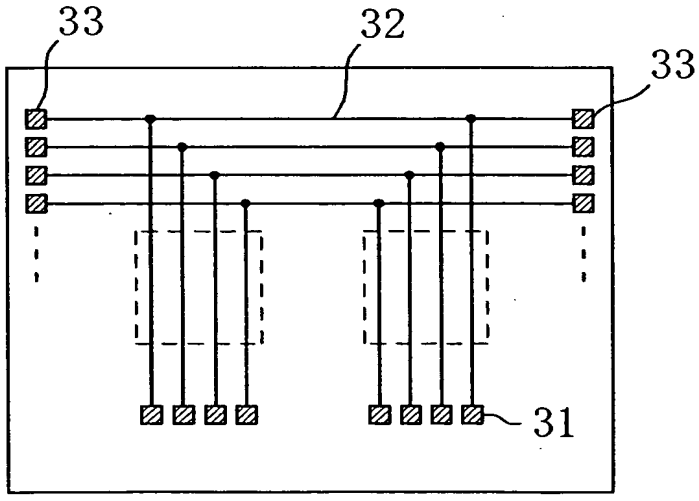

FIG. 6A

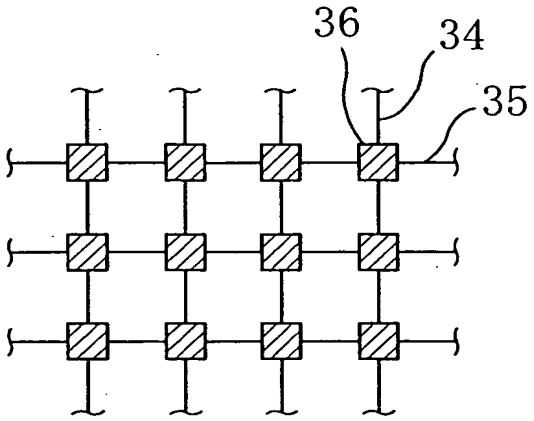

FIG. 6B

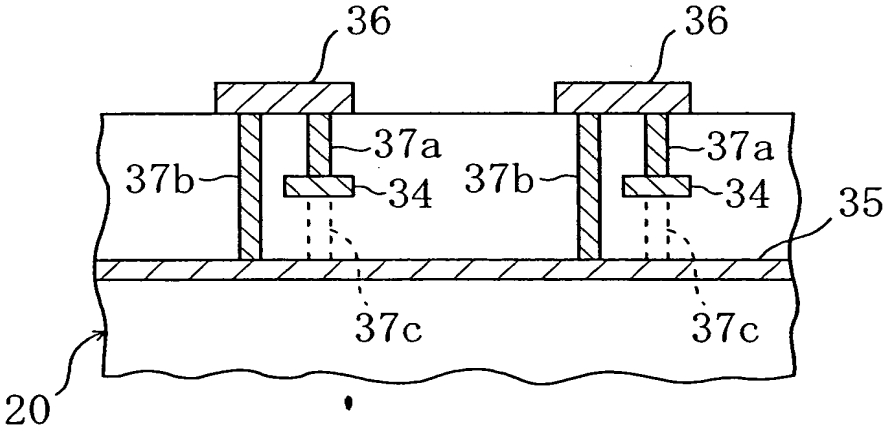

FIG. 7

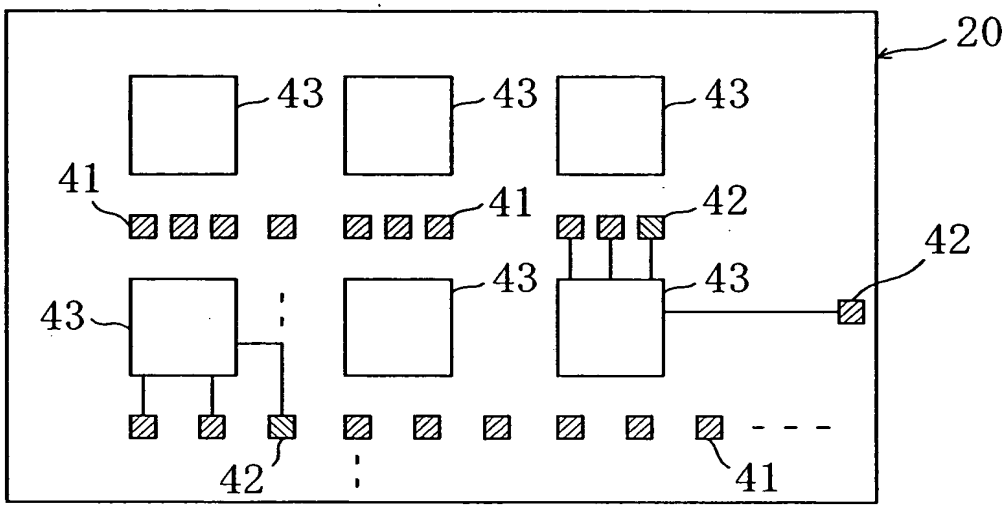

FIG. 8

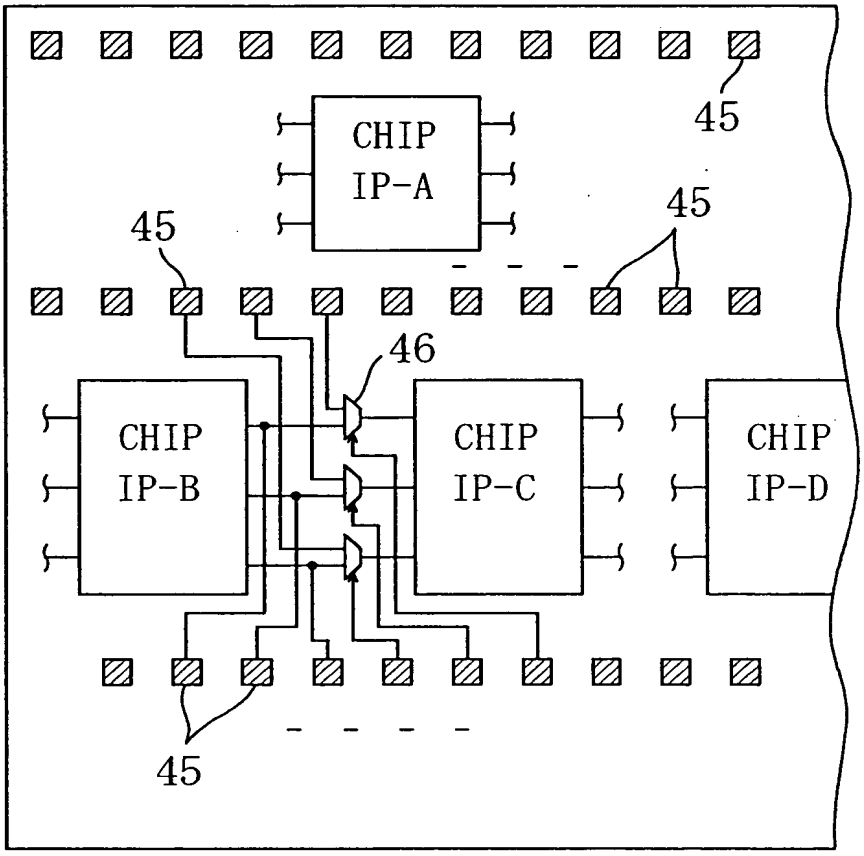

FIG. 9A

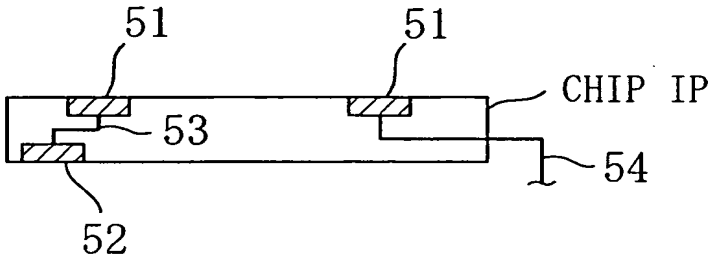
51
51
CHIP IP
53
54
52

FIG. 9B

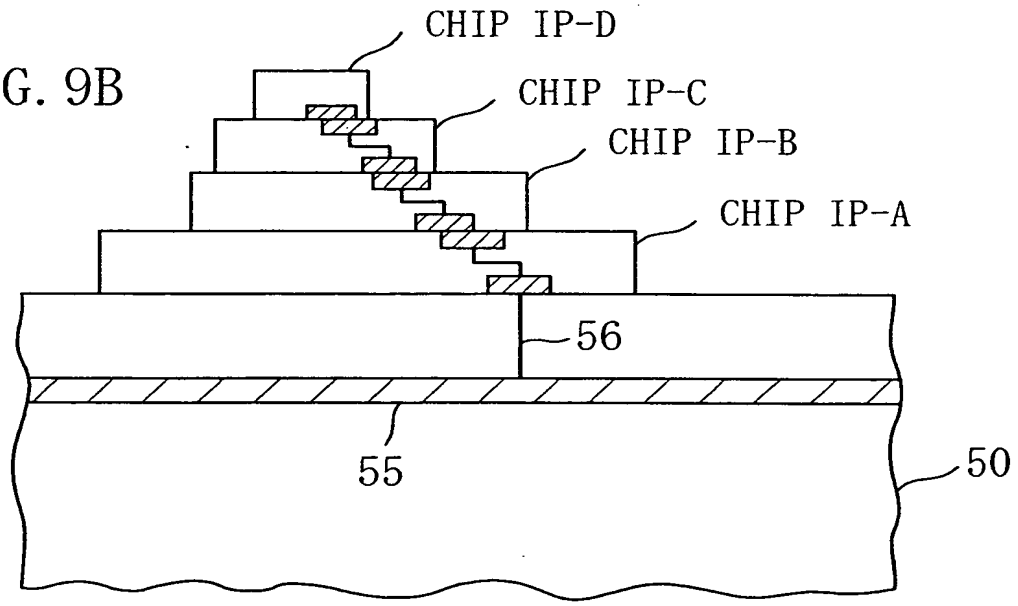
CHIP IP-D
CHIP IP-C
CHIP IP-B
CHIP IP-A
56
55
50

FIG. 10

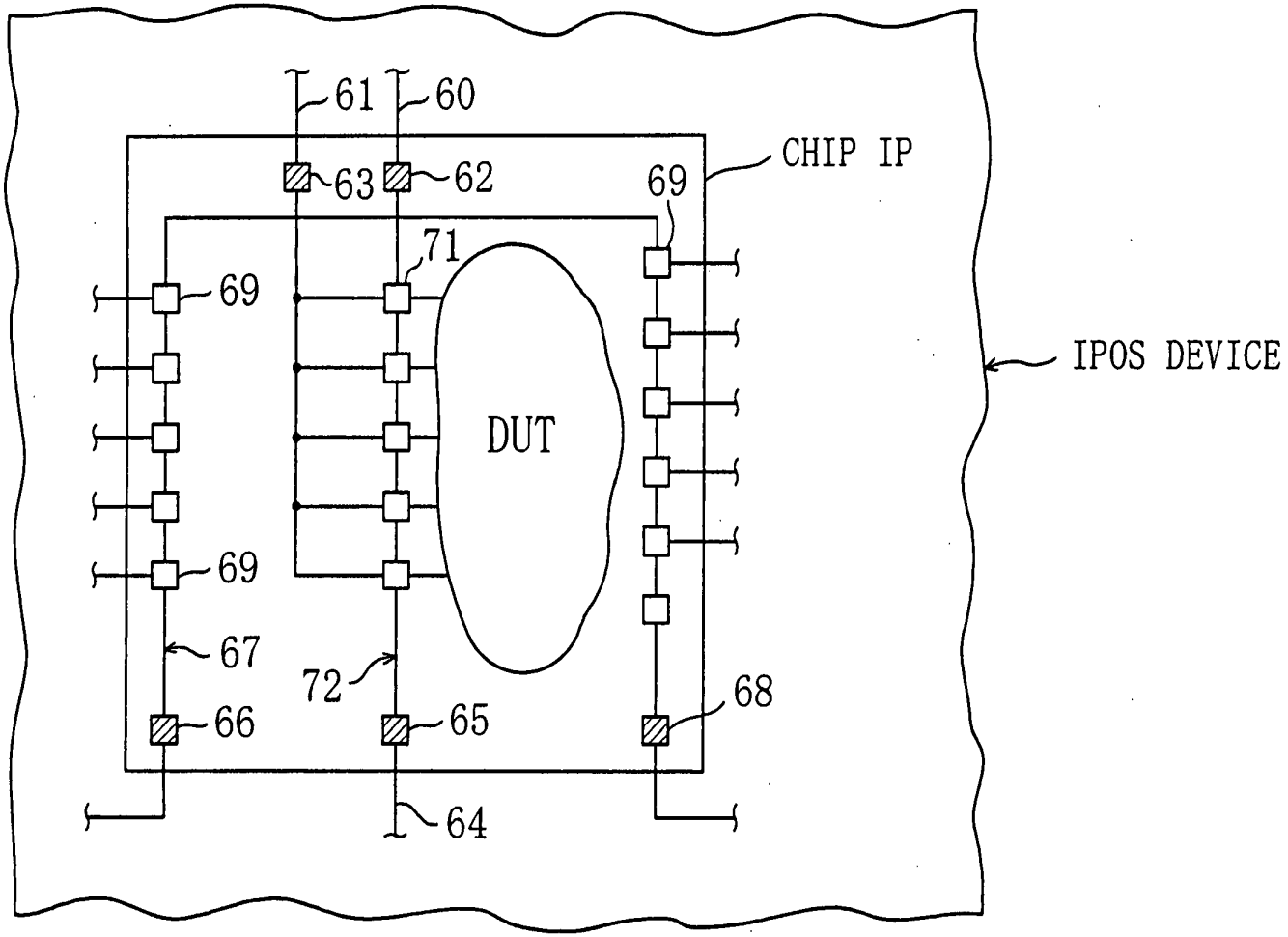

FIG. 11

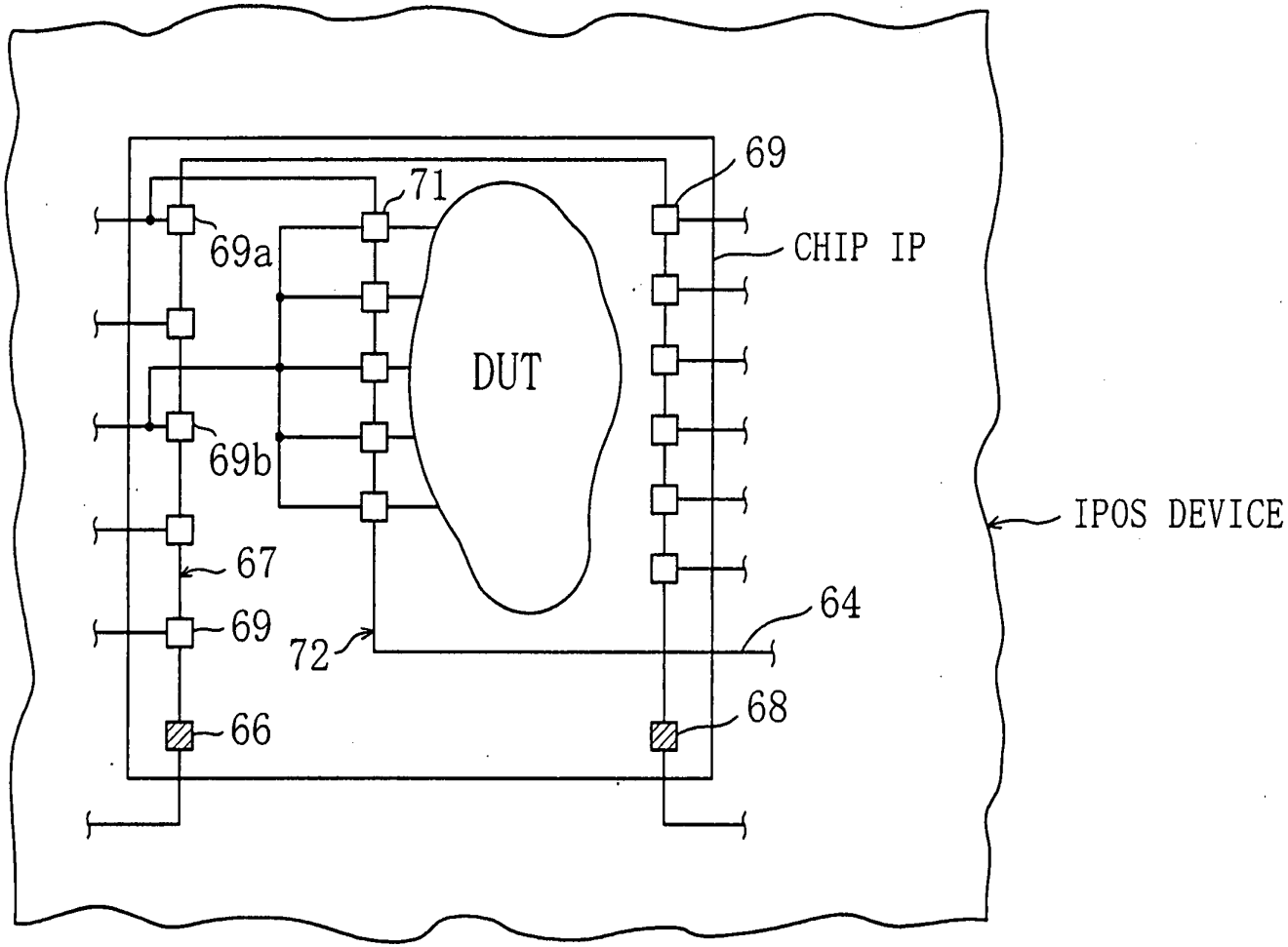

FIG. 12

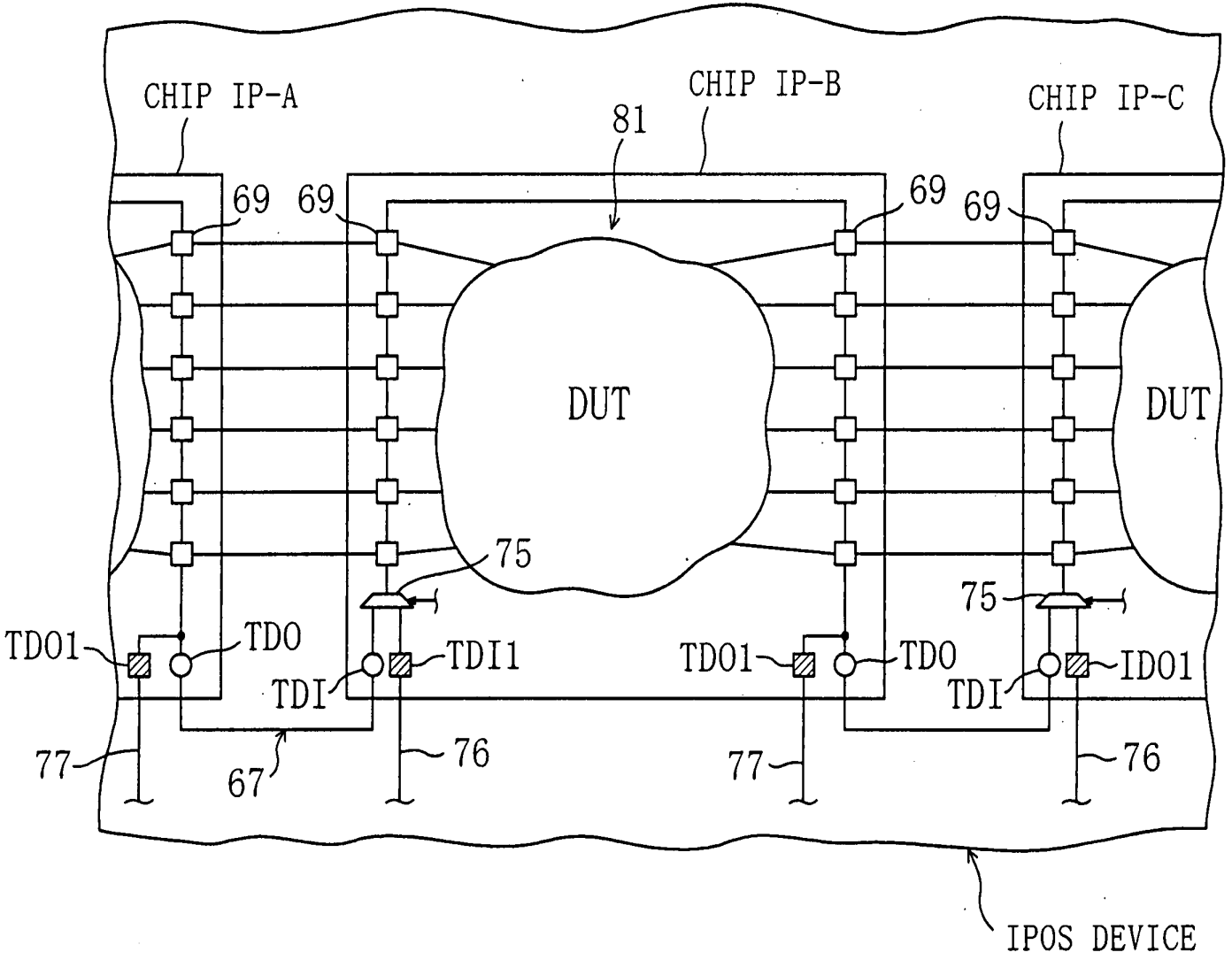
CHIP IP-A
CHIP IP-B
CHIP IP-C
81
69
69
69
69
DUT
DUT
75
75
TDO1
TDO
TDI1
TDI
TDO1
TDO
TDI
IDO1
77
67
76
77
76
IPOS DEVICE

FIG. 13

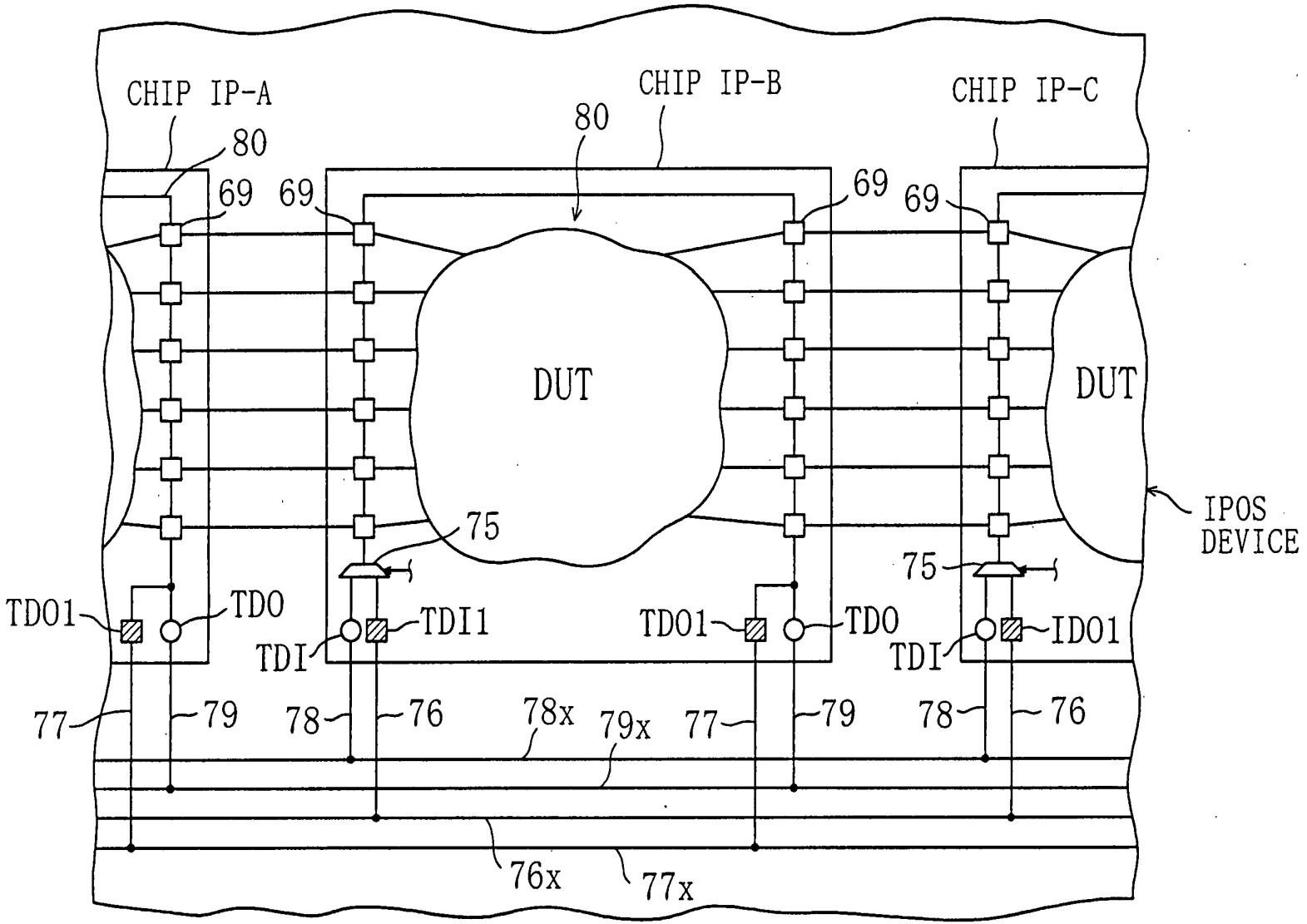
CHIP IP-A
CHIP IP-B
CHIP IP-C
80
80
69
69
69
69
DUT
DUT
IPOS
DEVICE
75
75
TDO1
TDO
TDI
TDI1
TDO1
TDO
TDI
IDO1
77
79
78
76
78x
79x
77
79
78
76
76x
77x

FIG. 14

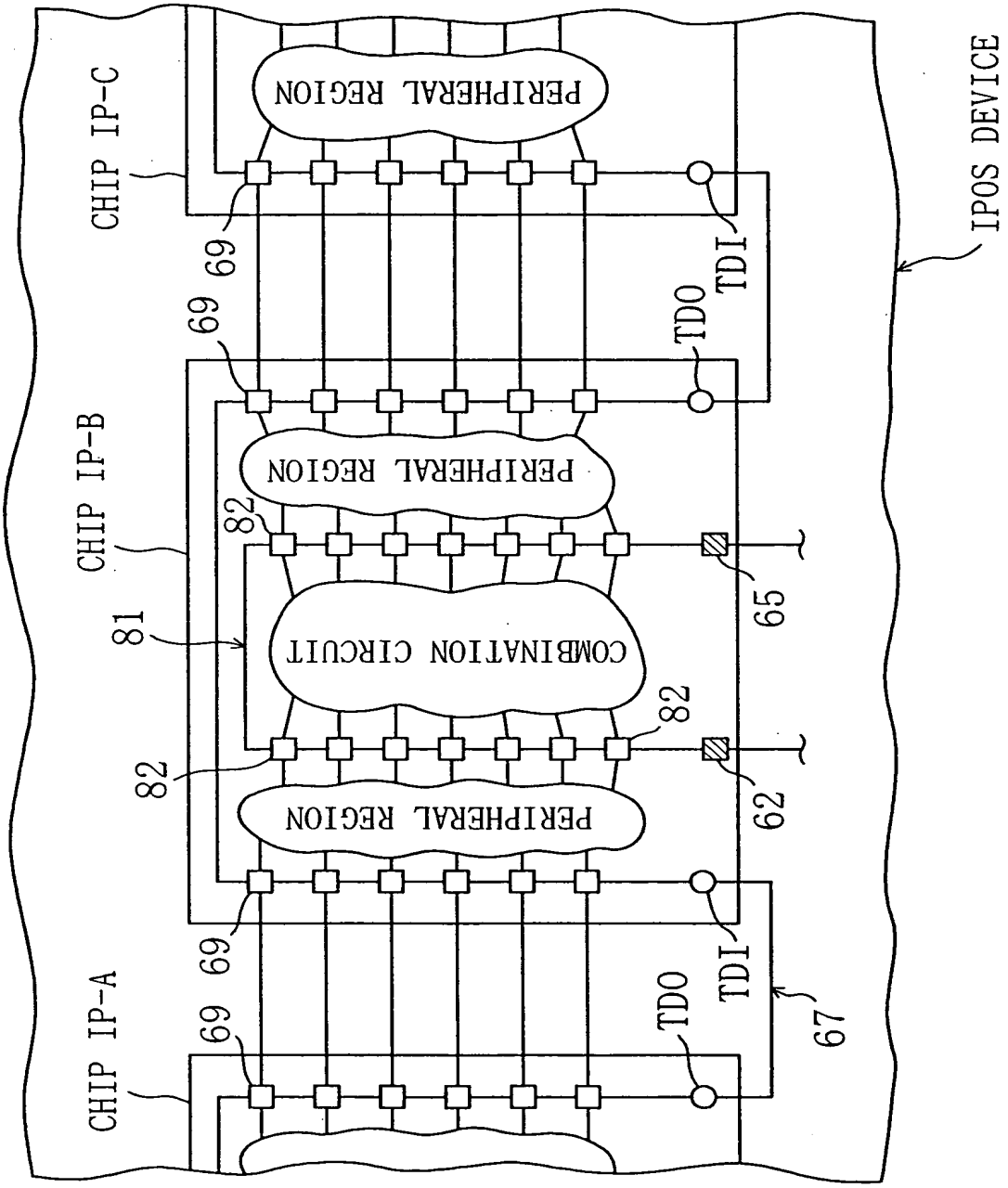
IPOS DEVICE
CHIP IP-C
CHIP IP-B
CHIP IP-A
PERIPHERAL REGION
PERIPHERAL REGION
COMBINATION CIRCUIT
PERIPHERAL REGION
69
69
69
69
TDI
TDO
TDI
TDO
82
82
82
81
65
62
67

FIG. 15

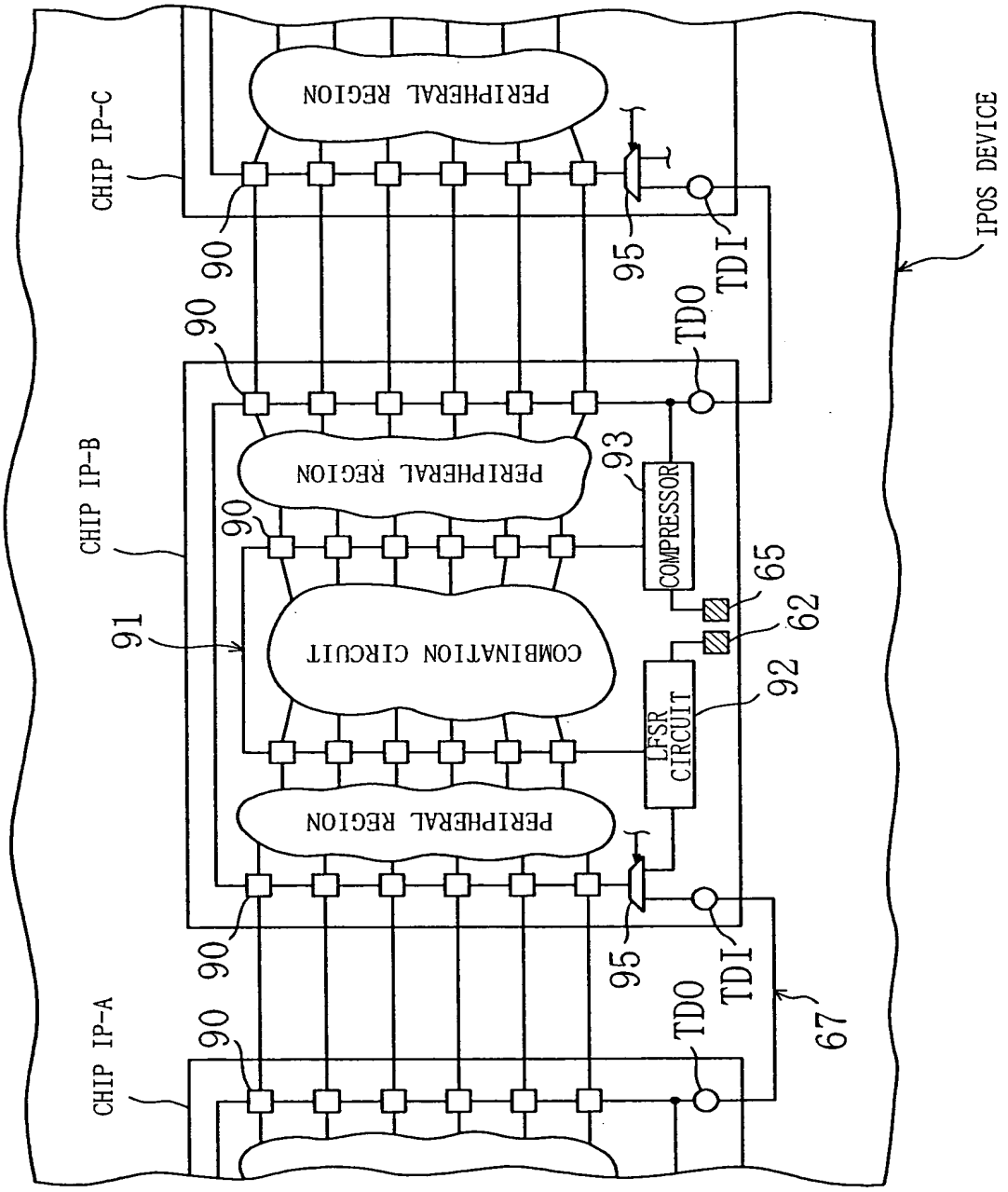
IPOS DEVICE
CHIP IP-C
CHIP IP-B
CHIP IP-A
PERIPHERAL REGION
PERIPHERAL REGION
PERIPHERAL REGION
COMBINATION CIRCUIT
COMPRESSOR
LFSR CIRCUIT
90
91
92
93
95
TDI
TDO
62
65
67

FIG. 16

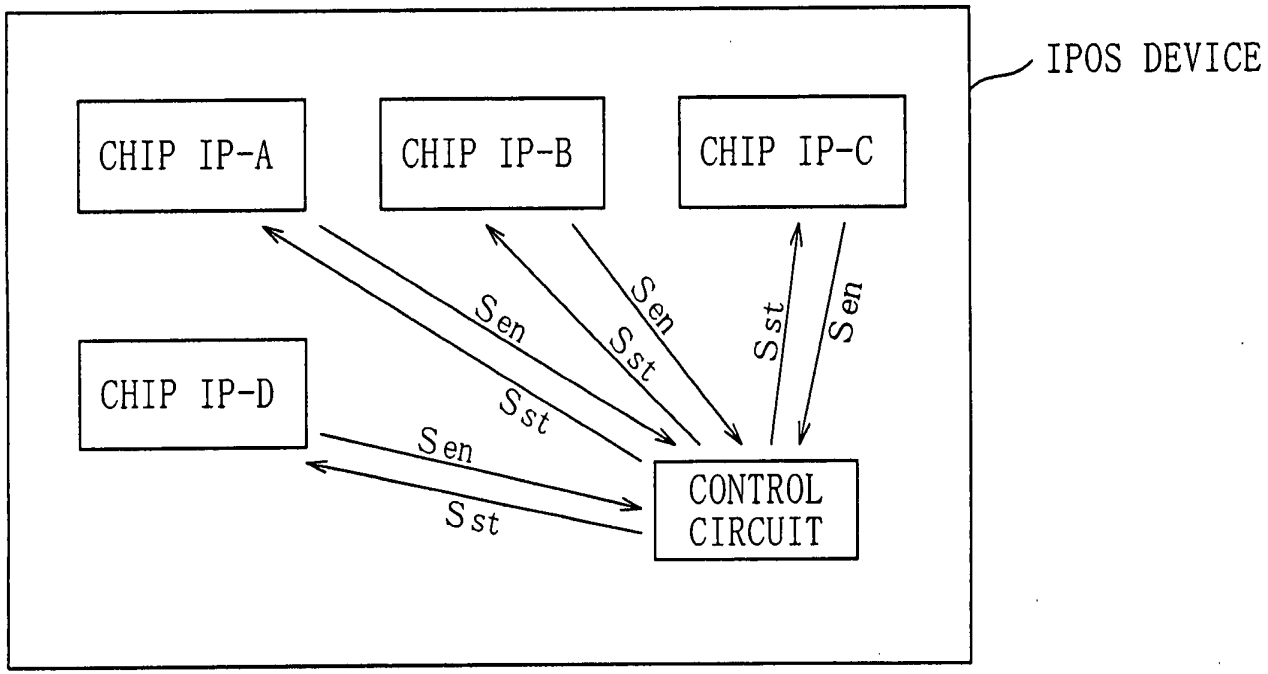
IPOS DEVICE
CHIP IP-A
CHIP IP-B
CHIP IP-C
CHIP IP-D
CONTROL CIRCUIT
Sen
Sst
Sen
Sst
Sst
Sen
Sen
Sst

FIG. 17A

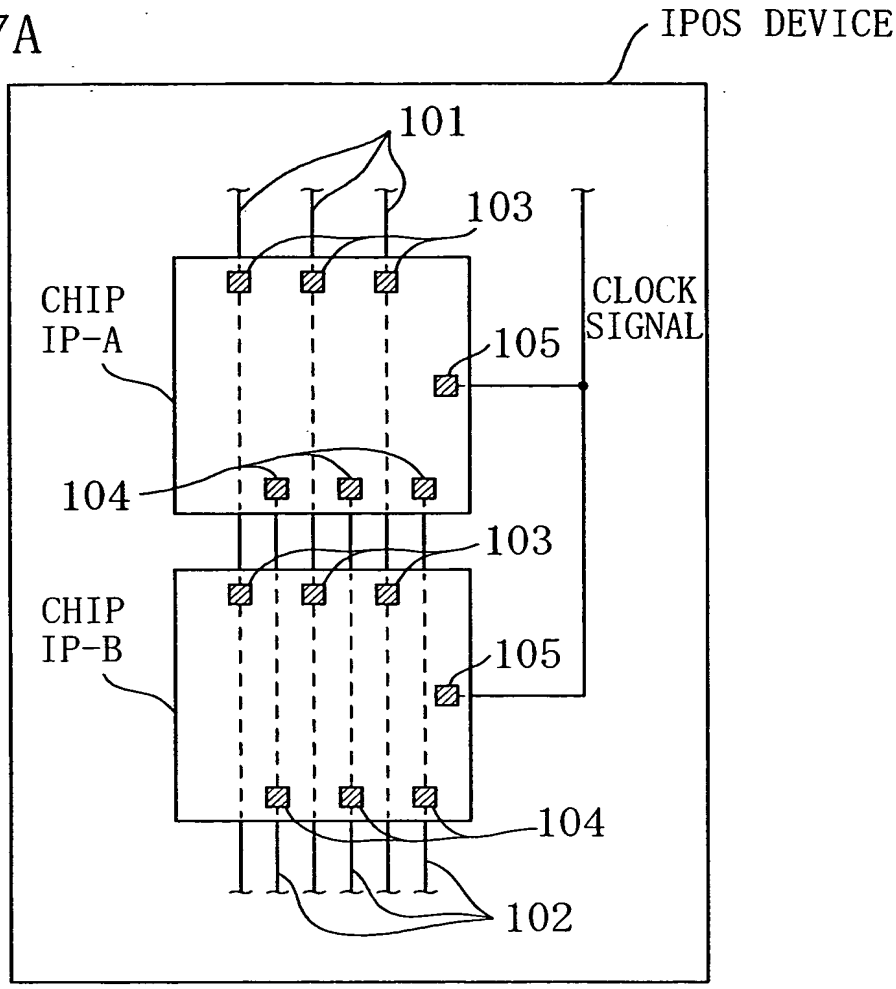

FIG. 17B

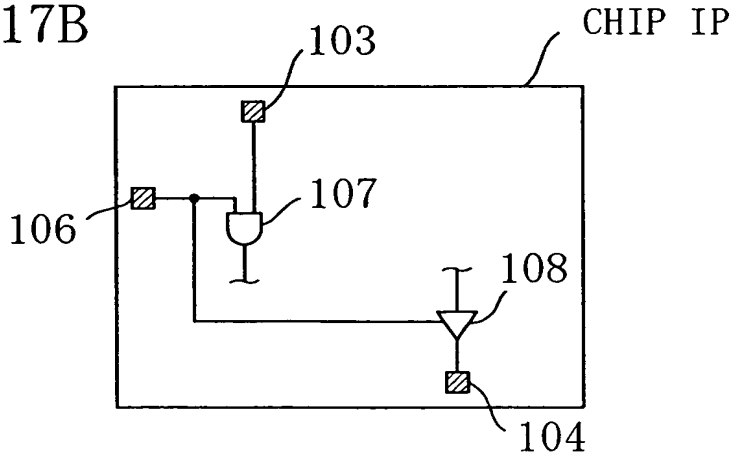

FIG. 18

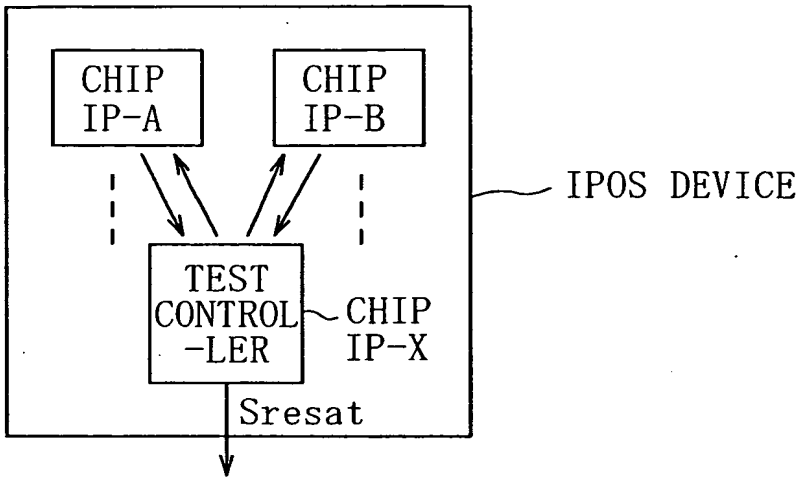
CHIP
IP-A
CHIP
IP-B
IPOS DEVICE
TEST
CONTROL
-LER
CHIP
IP-X
Sresat

FIG. 19

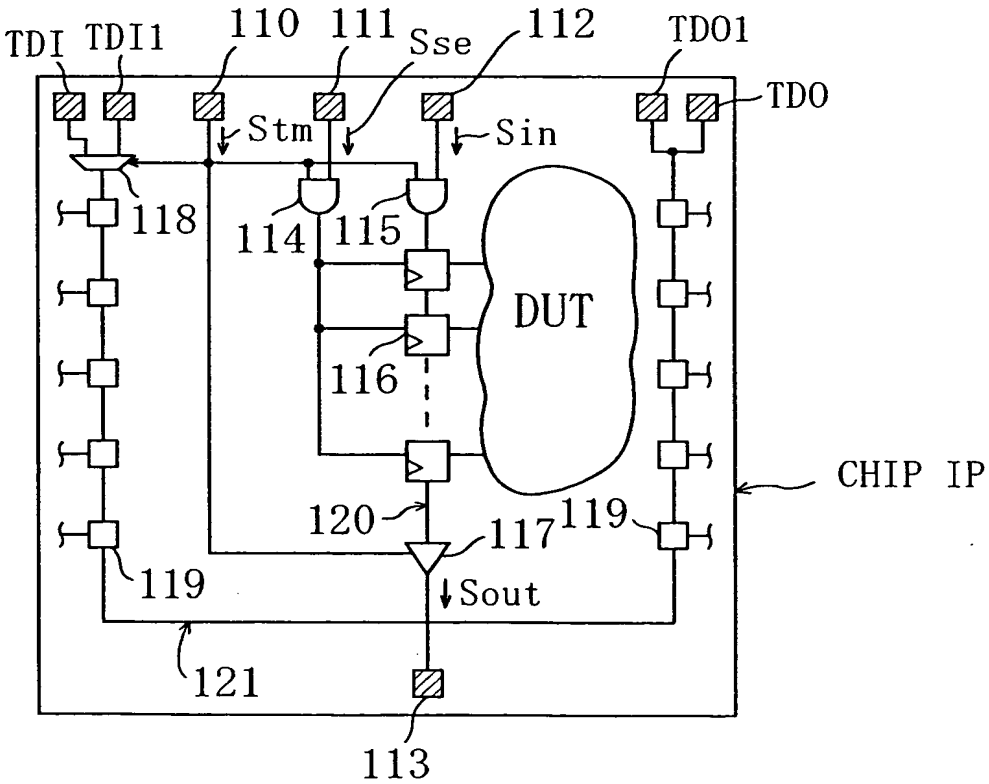
TDI
TDI1
110
111
Sse
112
TDO1
TDO
Stm
Sin
118
114
115
DUT
116
CHIP IP
120
117
119
119
Sout
121
113

FIG. 20

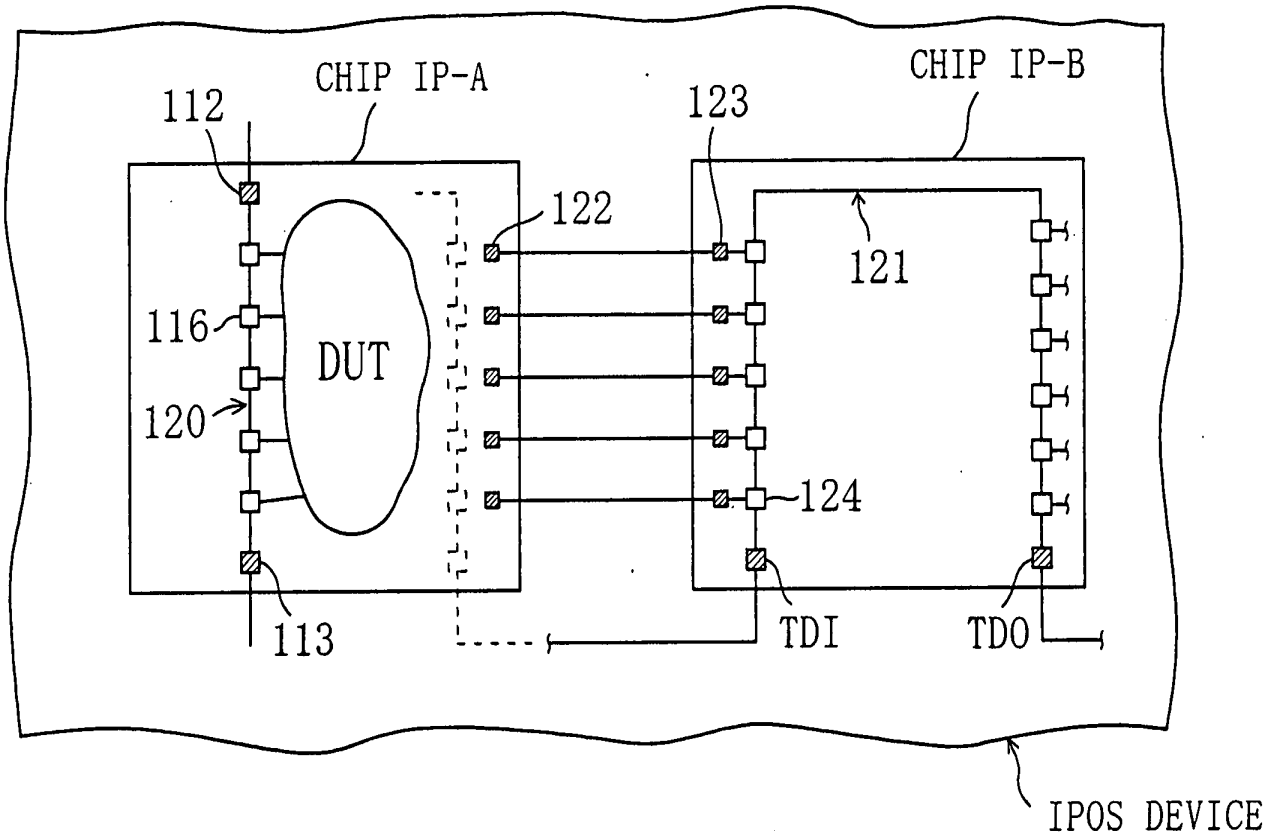
CHIP IP-A
CHIP IP-B
112
123
122
121
116
DUT
120
124
113
TDI
TDO
IPOS DEVICE

FIG. 21

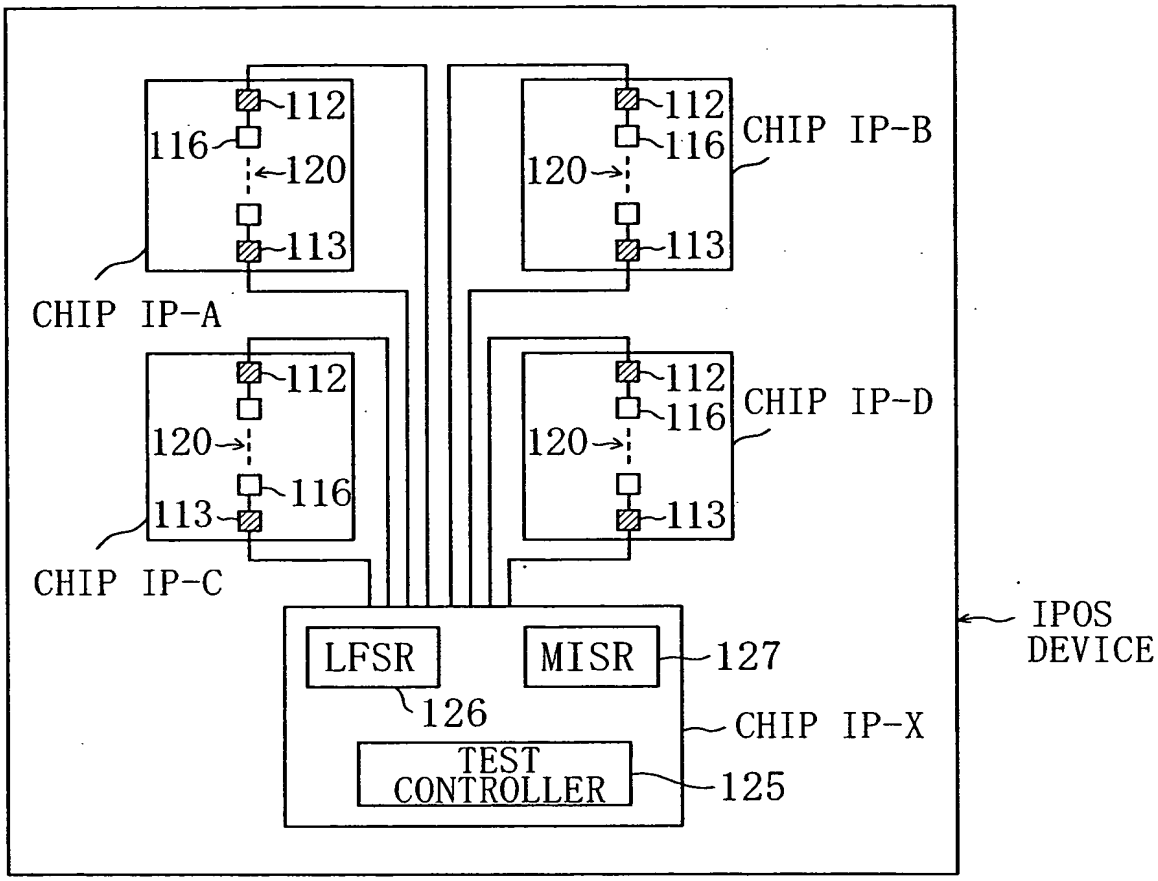
112
116
120
113
CHIP IP-A
112
116
120
CHIP IP-B
113
112
120
116
CHIP IP-C
113
112
116
120
CHIP IP-D
113
LFSR
MISR
127
126
CHIP IP-X
TEST CONTROLLER
125
IPOS DEVICE

FIG. 22A

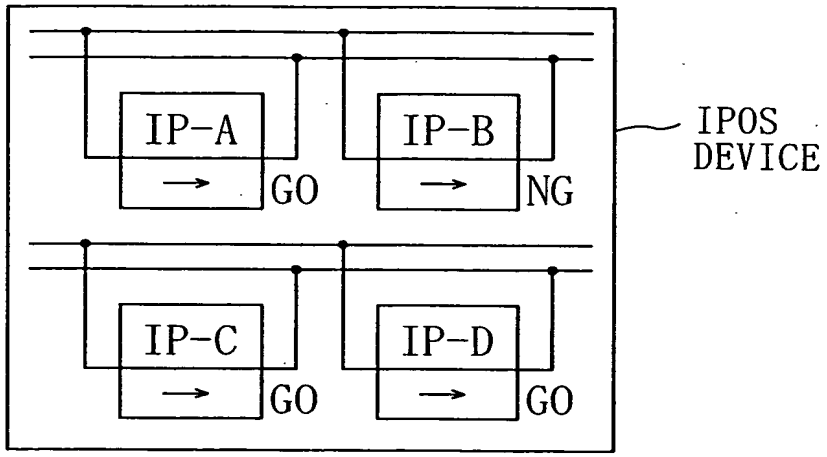

FIG. 22B

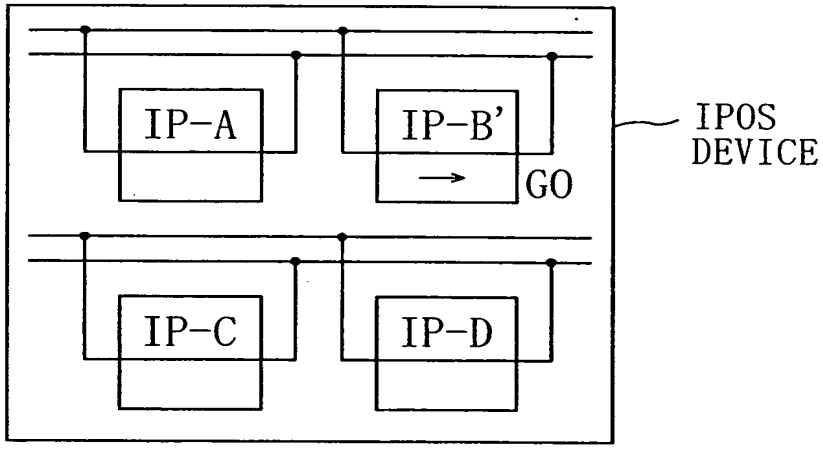

FIG. 23A

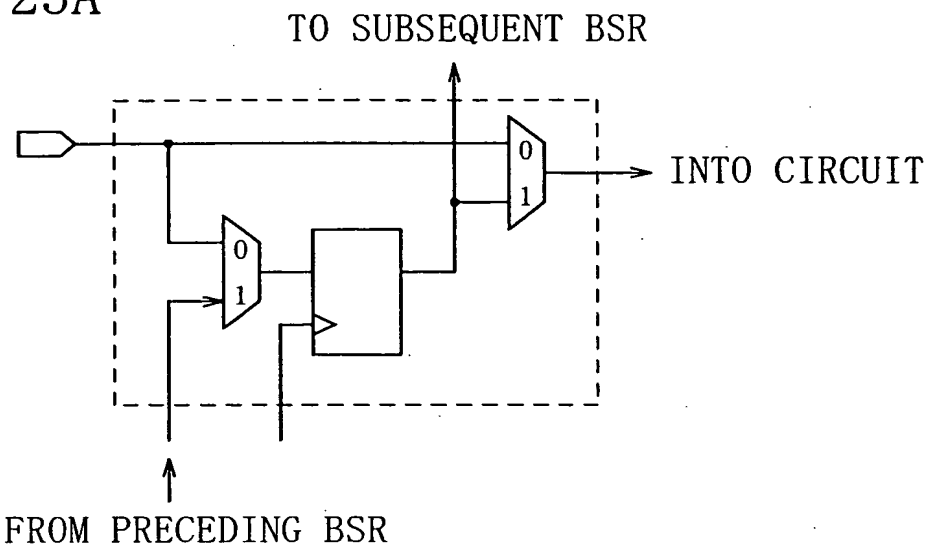

FIG. 23B

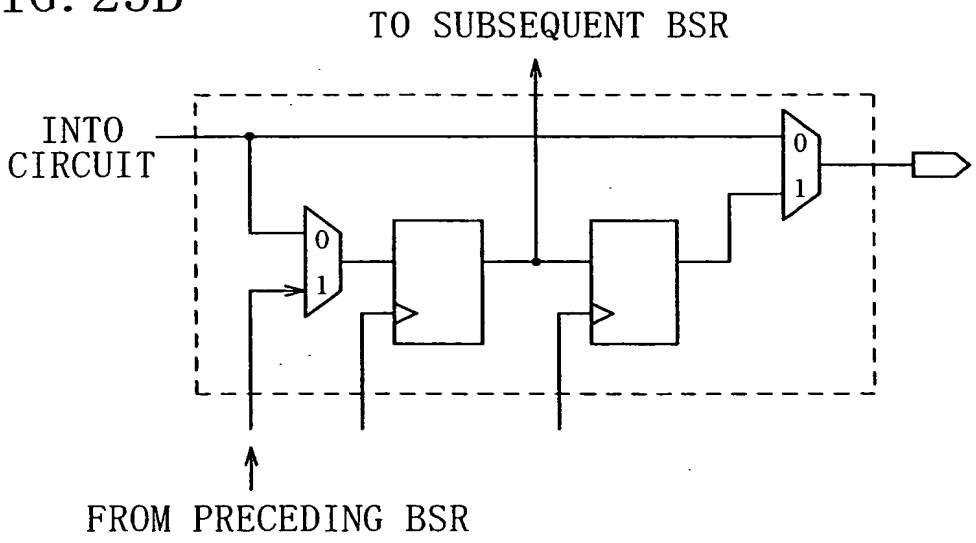

FIG. 24 PRIOR ART

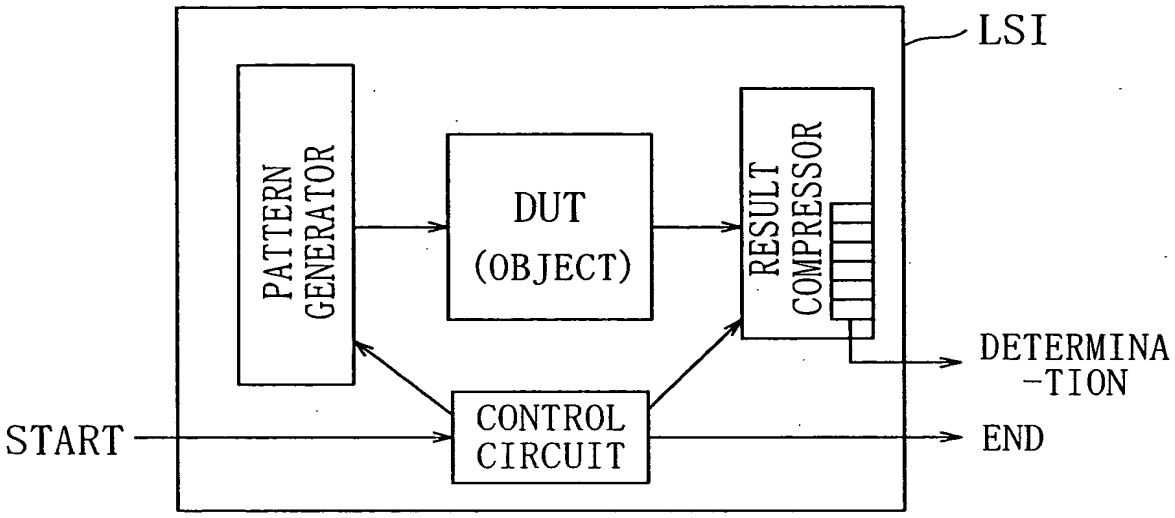

FIG. 25 PRIOR ART

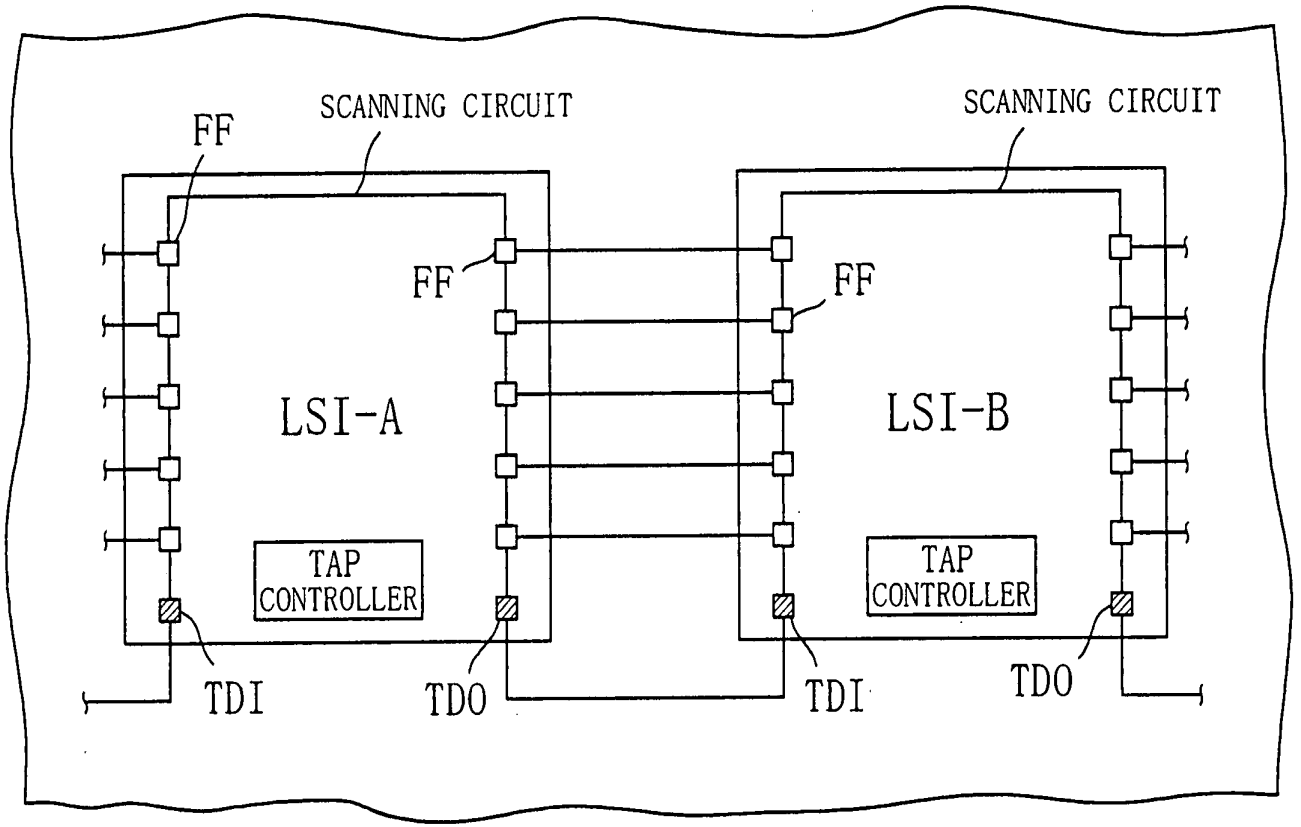

FIG. 26 PRIOR ART

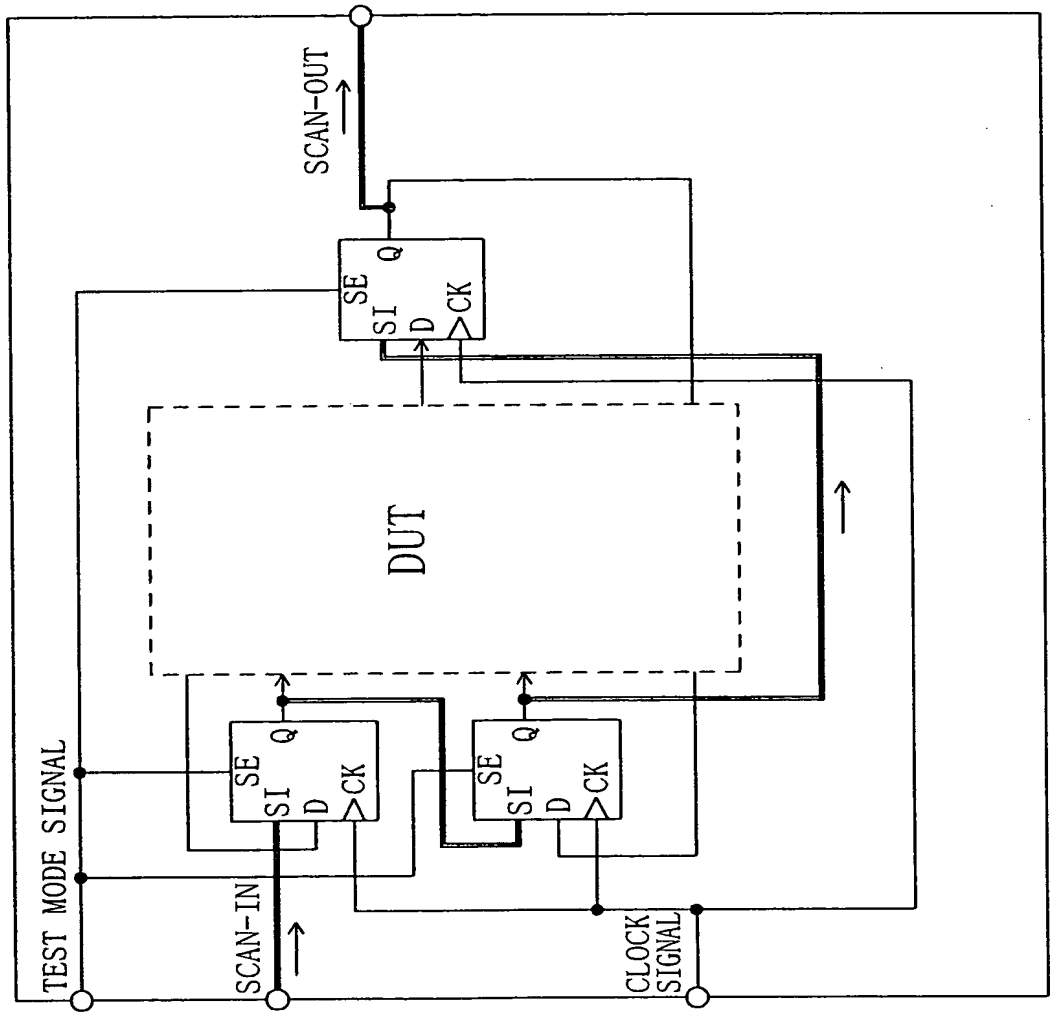
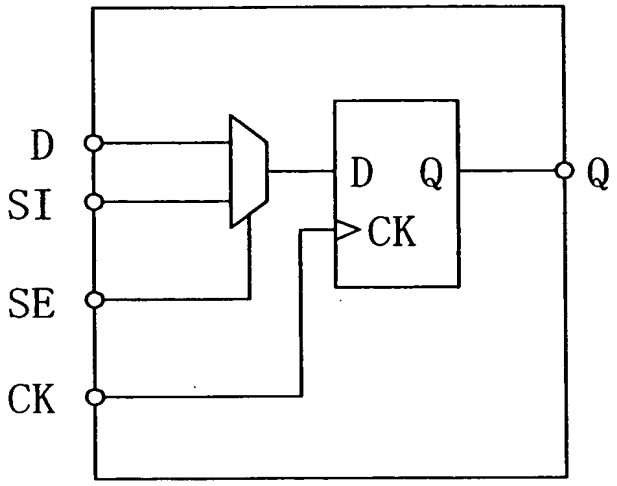
FIG. 27 PRIOR ART